ABSTRACT

A double layered low dielectric constant material dual damascene metallization process is described. Metal lines are provided covered by an insulating layer overlying a semiconductor substrate. A first organic dielectric layer is deposited overlying the insulating layer. A second inorganic dielectric layer is deposited overlying the first dielectric layer. In a first method, a via pattern is etched into the second dielectric layer. The via pattern is etched into the first dielectric layer using the patterned second dielectric layer as a mask. Thereafter, a trench pattern is etched into the second inorganic dielectric layer to complete dual damascene openings. In a second method, a trench pattern is etched into the second dielectric layer. Thereafter, a via pattern is etched through the second inorganic dielectric layer and the first organic dielectric layer to complete dual damascene openings. In a third method, a via pattern is etched into the second dielectric layer. Then, simultaneously, the via pattern is etched into the first dielectric layer and a trench pattern is etched into the second inorganic dielectric layer to complete dual damascene openings in the fabrication of an integrated circuit device.